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MS-7846

mATX
Ver: 2.1

Intel Sharkbay plamform H81 COLAY B85 H87

CPU:

INTEL-Haswell LGA1150

System Chipset:

H81,B85,H87

Memory:

DDRIII (1333/1666MHz) * 2 (Dual Channel)

PWM:

VRD12 - ISL95812

OnBoard Chipset:

HD Audio Codec:RTL887

LAN-realtek8111G

SIO:NUVOTON 6779D

SPI ROM: 64 MB & 128MB

Expansion Slots:

PCI Express (X16) Slot * 1

PCI Express (X1) Slot * 2

Other:

VGA*1

SATA2*2

SATA3*2

FRONT USB2.0 *4

FRONT USB3.0 *2

REAL USB2.0 *2

REAL USB3.0 *2

PS2*1

FRONT COM PORT*1

REAL PRINT PORT*1

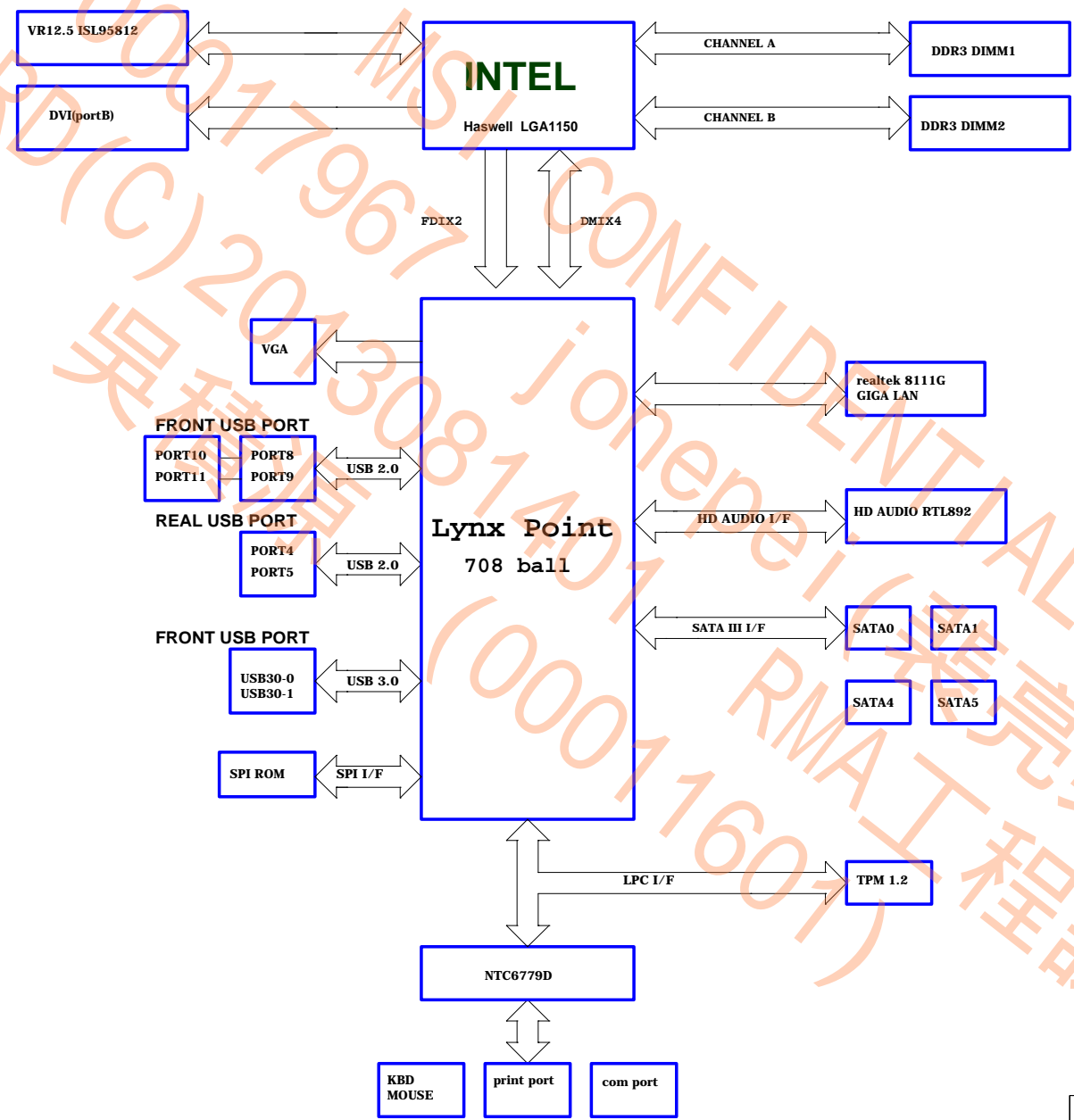


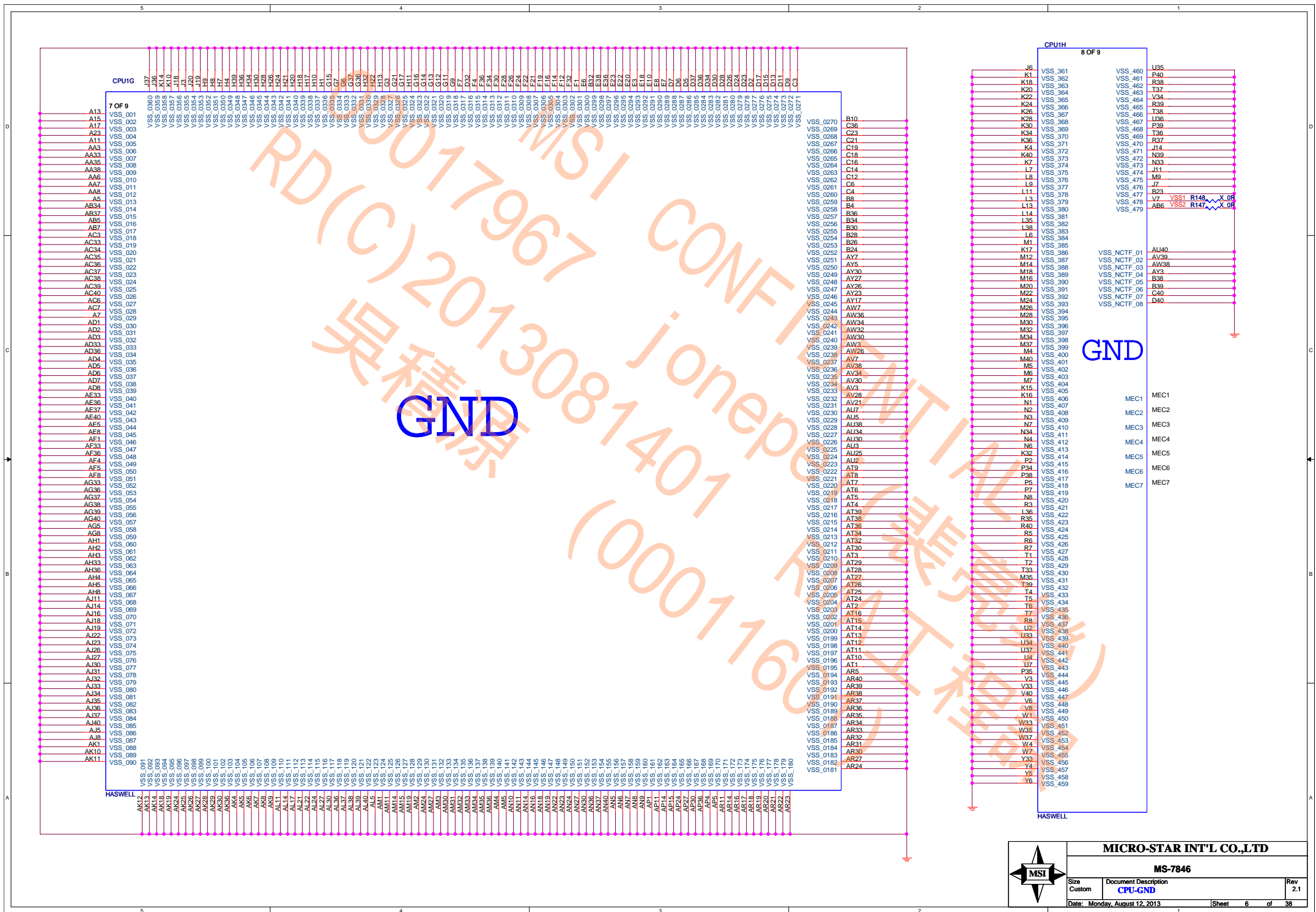
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MS-7846 Block Diagram





4 MEM_MA_DATA[63..0] << MEM_MA_DATA[63..0]

MEM_MA_DATA0 3
MEM_MA_DATA1 4
MEM_MA_DATA2 9
MEM_MA_DATA3 10
MEM_MA_DATA4 122
MEM_MA_DATA5 123
MEM_MA_DATA6 128
MEM_MA_DATA7 129
MEM_MA_DATA8 12
MEM_MA_DATA9 13
MEM_MA_DATA10 18
MEM_MA_DATA11 19
MEM_MA_DATA12 131
MEM_MA_DATA13 132
MEM_MA_DATA14 137
MEM_MA_DATA15 138
MEM_MA_DATA16 21
MEM_MA_DATA17 22
MEM_MA_DATA18 27
MEM_MA_DATA19 28
MEM_MA_DATA20 140
MEM_MA_DATA21 141
MEM_MA_DATA22 146
MEM_MA_DATA23 147
MEM_MA_DATA24 30
MEM_MA_DATA25 31
MEM_MA_DATA26 36
MEM_MA_DATA27 37
MEM_MA_DATA28 149
MEM_MA_DATA29 150
MEM_MA_DATA30 155
MEM_MA_DATA31 156
MEM_MA_DATA32 81
MEM_MA_DATA33 82
MEM_MA_DATA34 87
MEM_MA_DATA35 88
MEM_MA_DATA36 200
MEM_MA_DATA37 201
MEM_MA_DATA38 206
MEM_MA_DATA39 207
MEM_MA_DATA40 90
MEM_MA_DATA41 91
MEM_MA_DATA42 96
MEM_MA_DATA43 97
MEM_MA_DATA44 209
MEM_MA_DATA45 210
MEM_MA_DATA46 215
MEM_MA_DATA47 216
MEM_MA_DATA48 99
MEM_MA_DATA49 100
MEM_MA_DATA50 105
MEM_MA_DATA51 106
MEM_MA_DATA52 218
MEM_MA_DATA53 219
MEM_MA_DATA54 224
MEM_MA_DATA55 225
MEM_MA_DATA56 108
MEM_MA_DATA57 109
MEM_MA_DATA58 114
MEM_MA_DATA59 115
MEM_MA_DATA60 227
MEM_MA_DATA61 228
MEM_MA_DATA62 233
MEM_MA_DATA63 234

DIMM1
VDD 51
VDD 54
VDD 57
VDD 58
VDD 62
VDD 65
VDD 66
VDD 72
VDD 75
VDD 76
VDD 176
VDD 177
VDD 178
VDD 183
VDD 186
VDD 188
VDD 189
VDD 194
VDD 197
VDD 236
VDDSPD 120
VTT 240
VTT 240
NC/PAIR_IN 68
NC/PAIR_OUT 53
NC/TEST4 127
NC/TEST5 128
FREE0 48
FREE1 49
FREE2 48
FREE3 49
FREE4 48

DDR3

MEM_MA_ADD0 188
MEM_MA_ADD1 181
MEM_MA_ADD2 61
MEM_MA_ADD3 180
MEM_MA_ADD4 59
MEM_MA_ADD5 58
MEM_MA_ADD6 178
MEM_MA_ADD7 56
MEM_MA_ADD8 177
MEM_MA_ADD9 175
MEM_MA_ADD10 70
MEM_MA_ADD11 55
MEM_MA_ADD12 174
MEM_MA_ADD13 198
MEM_MA_ADD14 172
MEM_MA_ADD15 171

MEM_MA_DQS_H0 7
MEM_MA_DQS_L0 6
MEM_MA_DQS_H1 16
MEM_MA_DQS_L1 15
MEM_MA_DQS_H2 25
MEM_MA_DQS_L2 24
MEM_MA_DQS_H3 34
MEM_MA_DQS_L3 33
MEM_MA_DQS_H4 85
MEM_MA_DQS_L4 84
MEM_MA_DQS_H5 94
MEM_MA_DQS_L5 93
MEM_MA_DQS_H6 103
MEM_MA_DQS_L6 102
MEM_MA_DQS_H7 112
MEM_MA_DQS_L7 111

MEM_MA_ODT0 195
MEM_MA_ODT1 77
MEM_MA_CKE0 50
MEM_MA_CKE1 169
MEM_MA_CS_L0 193
MEM_MA_CS_L1 76
MEM_MA_BANK0 71
MEM_MA_BANK1 190
MEM_MA_BANK2 52

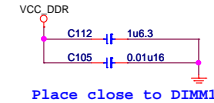
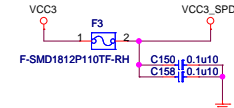
MEM_MA_WE_L 73
MEM_MA_RAS_L 192
MEM_MA_CAS_L 74
MEM_MA_DRAMRST# 168
MEM_MA_CLK_H0 184
MEM_MA_CLK_L0 185
MEM_MA_CLK_H1 63
MEM_MA_CLK_L1 64

VREF_DQ_A 1
VREF_CA_A 67
SMBCLK_DDR 118
SMBDATA_DDR 238
SMBCLK_VCC 11,28,33
SMBDATA_VCC 11,28,33

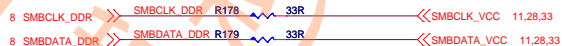
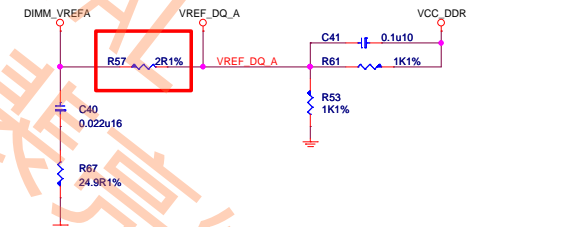
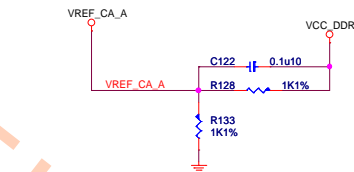
MEM_MA_CLK_H0 184
MEM_MA_CLK_L0 185
MEM_MA_CLK_H1 63
MEM_MA_CLK_L1 64


DIMM1 (CHANNEL-A)
ADDRESS = 0:0 [SA1:SA0]

DDR3-240P_BLACK-RH-24



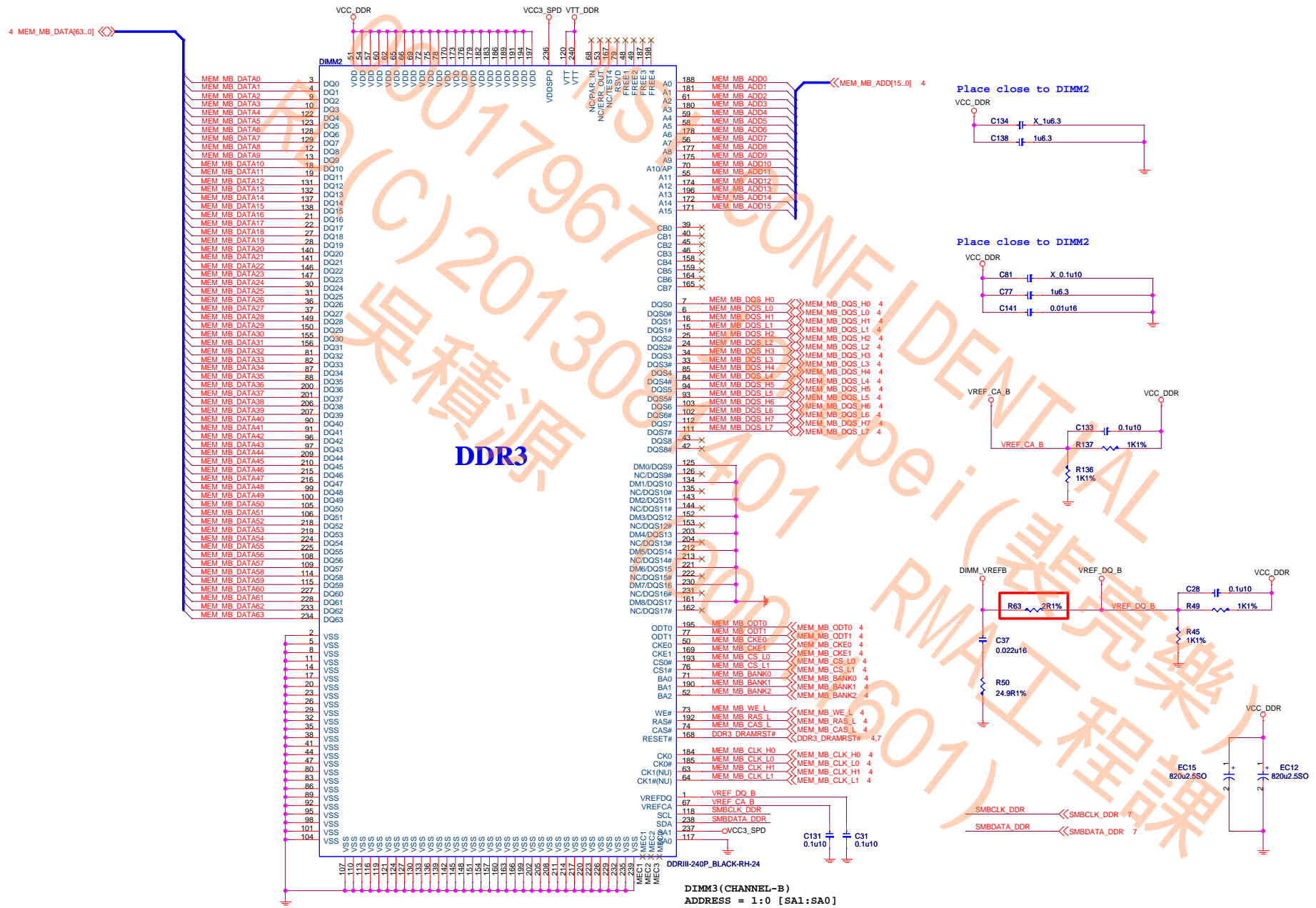
Place close to DIMM1



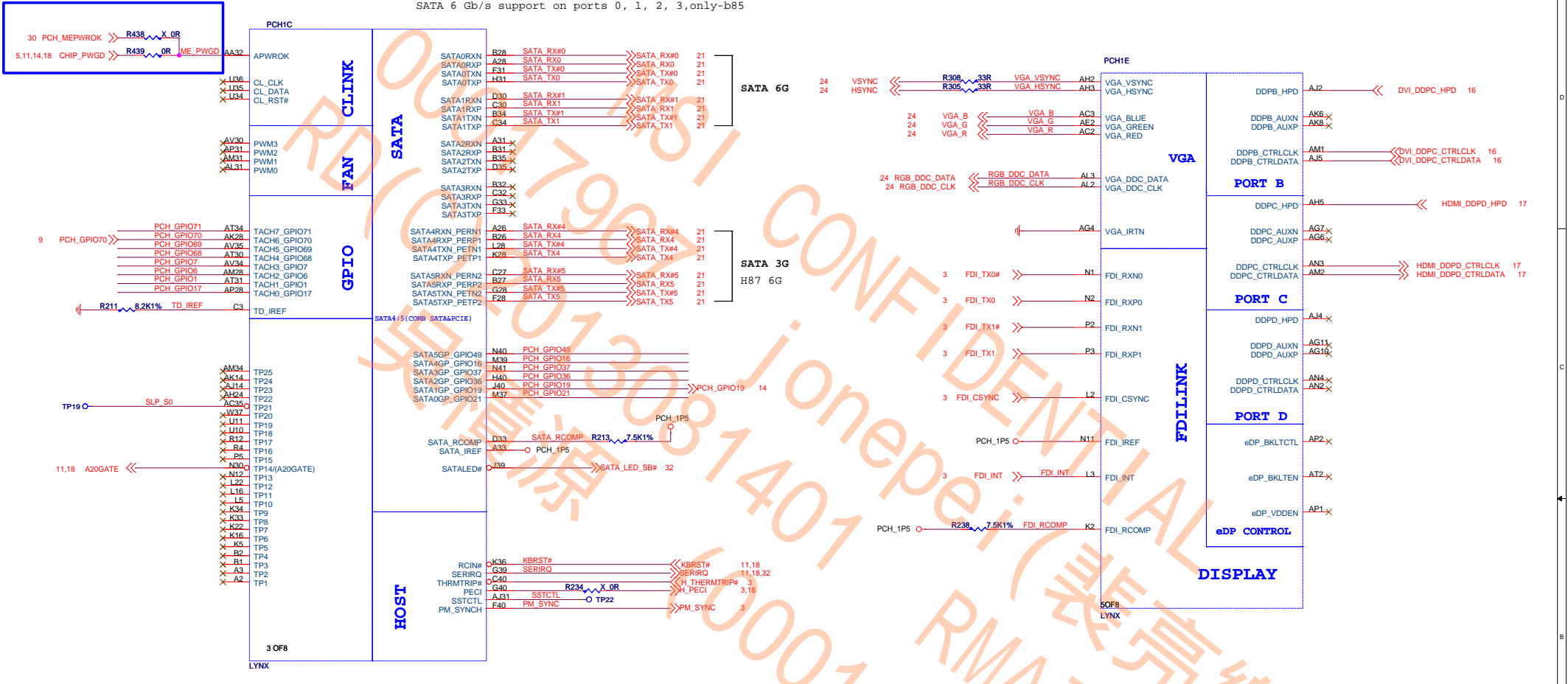


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Size Custom	Document Description DDR3 Chane-A DIMM1/2	Rev 2.1
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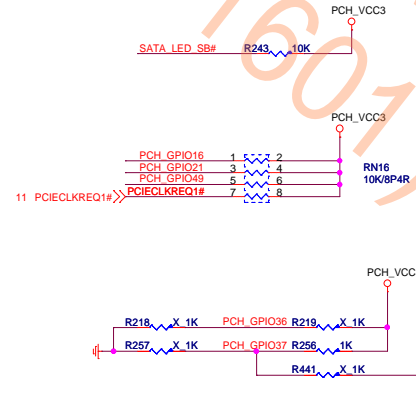
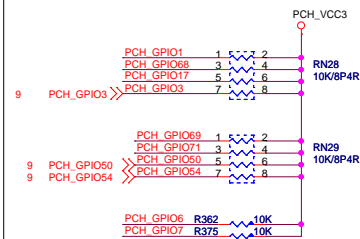
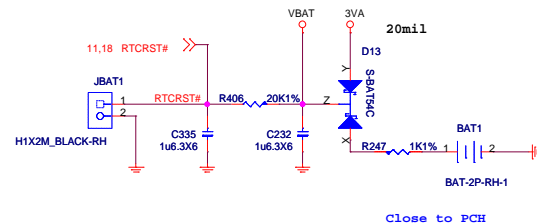
DDRIII DIMM_B0



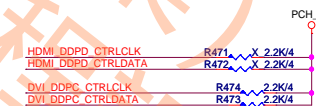
SATA 6 Gb/s support on ports 0 and 1 only.-h81
SATA 6 Gb/s support on ports 0, 1, 2, 3, 4, 5, 6 only-h87
SATA 6 Gb/s support on ports 0, 1, 2, 3,only-b85



RTC and CLR_CMOS



Enable VGA(CTRLCLK/DATA Pull High)



Close to PCH within 250mils.



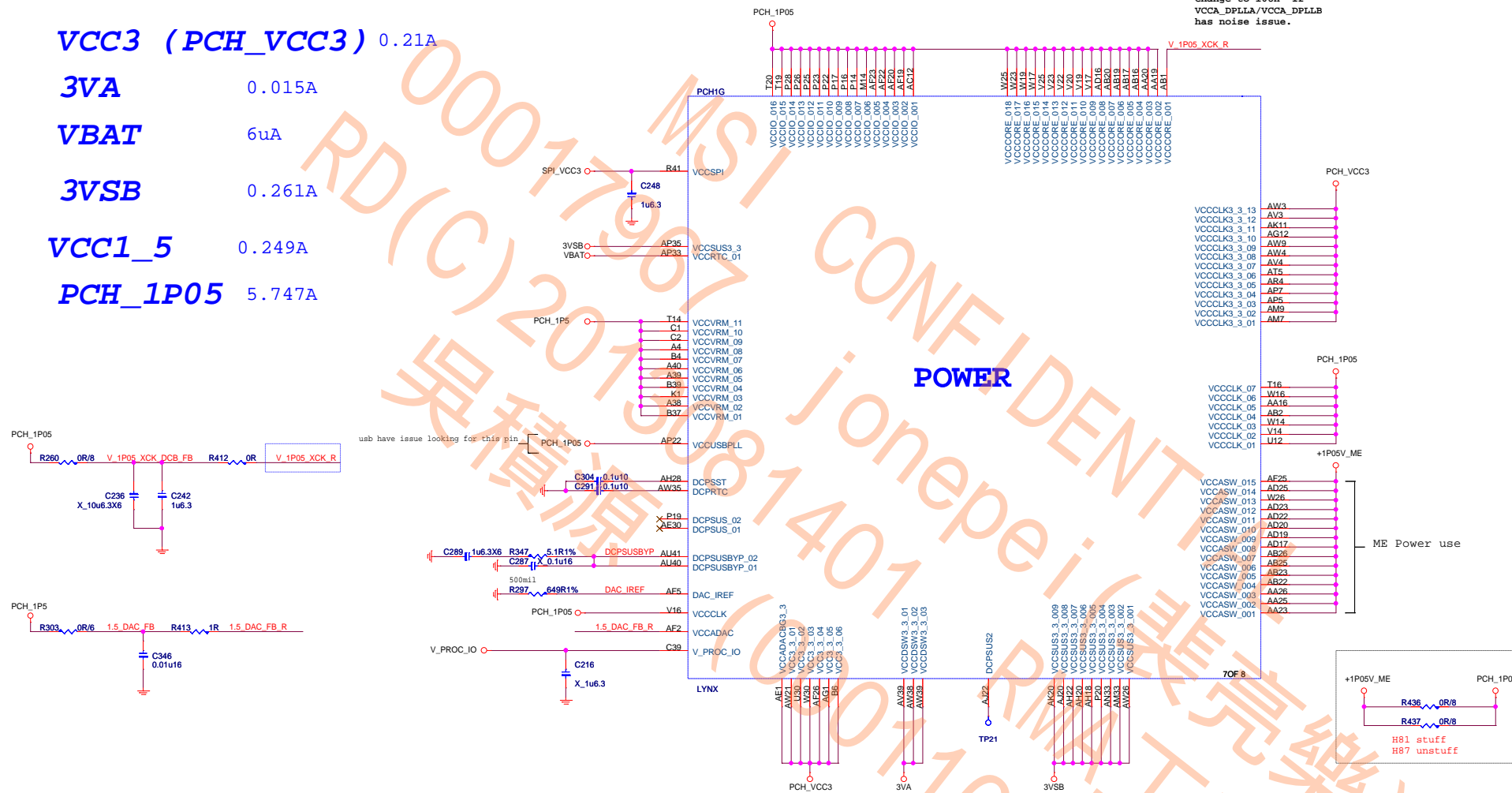
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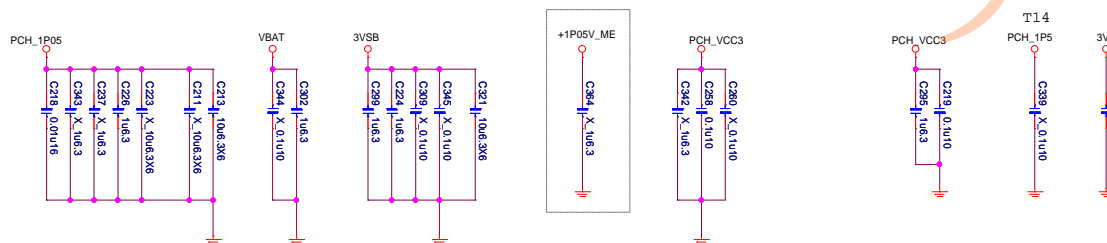
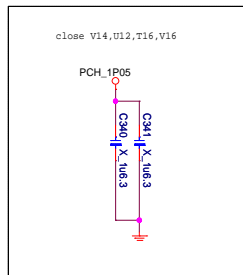
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PCH 1P05 5.747A

POWER



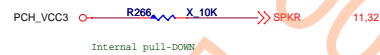
PCH VCC3 HAVE SEOENCING



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PCH Straps



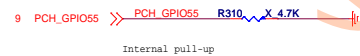
SPKR

Default Mode:

Internal weak Pull-down.

No Reboot Mode with TCO Disabled:

Connect to Vcc3_3 with 8.2k-10k Ohm weak pullup resistor.



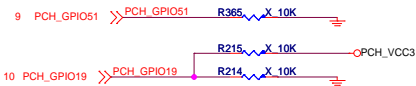
GPIO55

Default Mode:

Internal pull-up.

Top Block Swap Mode:

Connect to ground with 4.7k Ohm weak pulldown resistor.



SATA1GP/GPIO19, GPIO51

Default (SPI):

Left both SATA1GP/GPIO19 and GPIO51 floating.
No pull up required.

Boot from PCI:

Connect SATA1GP/GPIO19 to ground with 1k Ohm pull-down resistor.
Leave GPIO51 Floating.

Boot from LPC:

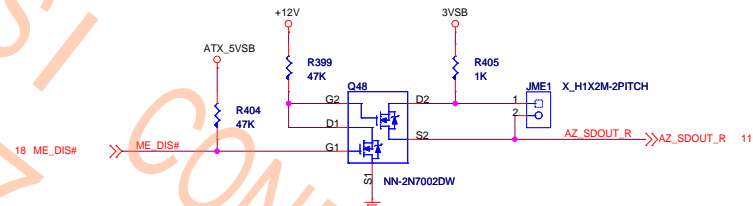
Connect both SATA1GP/GPIO19 and GPIO51 to ground with 1k Ohm pull-down resistor.



GPIO53

Do not pull low.

Connect to ground with 1k Ohm pull-down resistor.

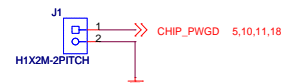


HDA_SDO

Default:
Do not pull high.

Disable ME in Manufacturing Mode:
Connect to VccSusHDA with 1k Ohm pull-up resistor through a jumper.

For test cpu voltage

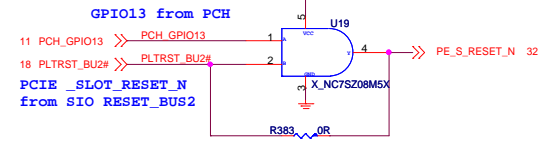
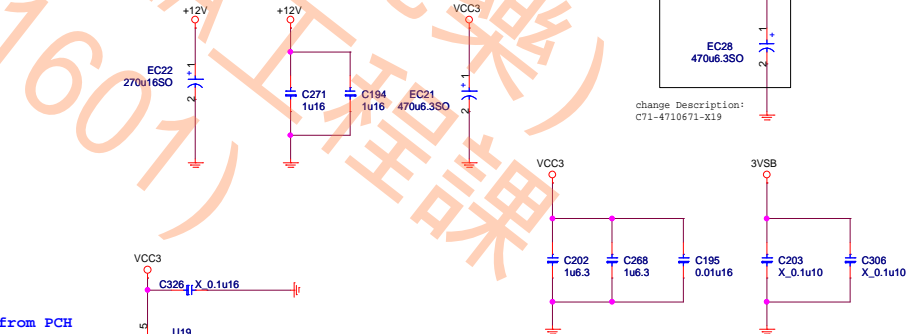
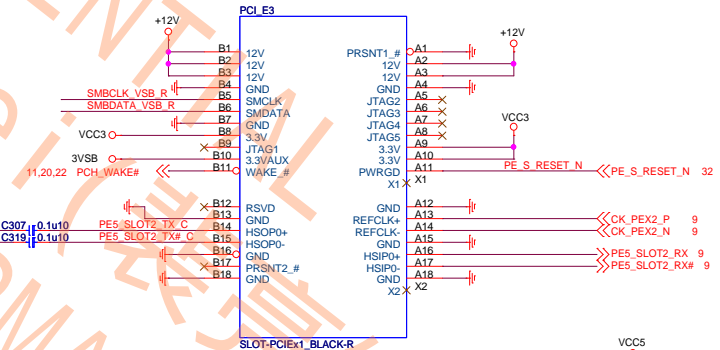
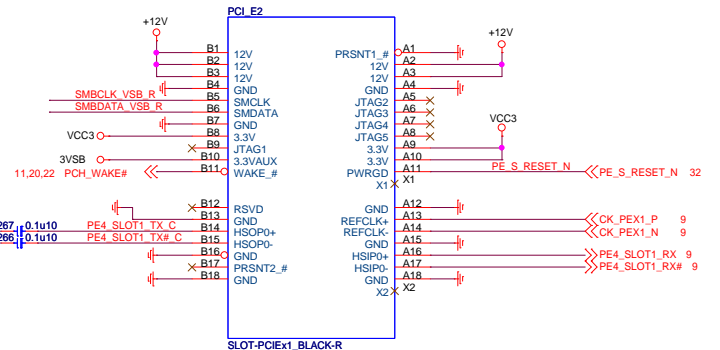
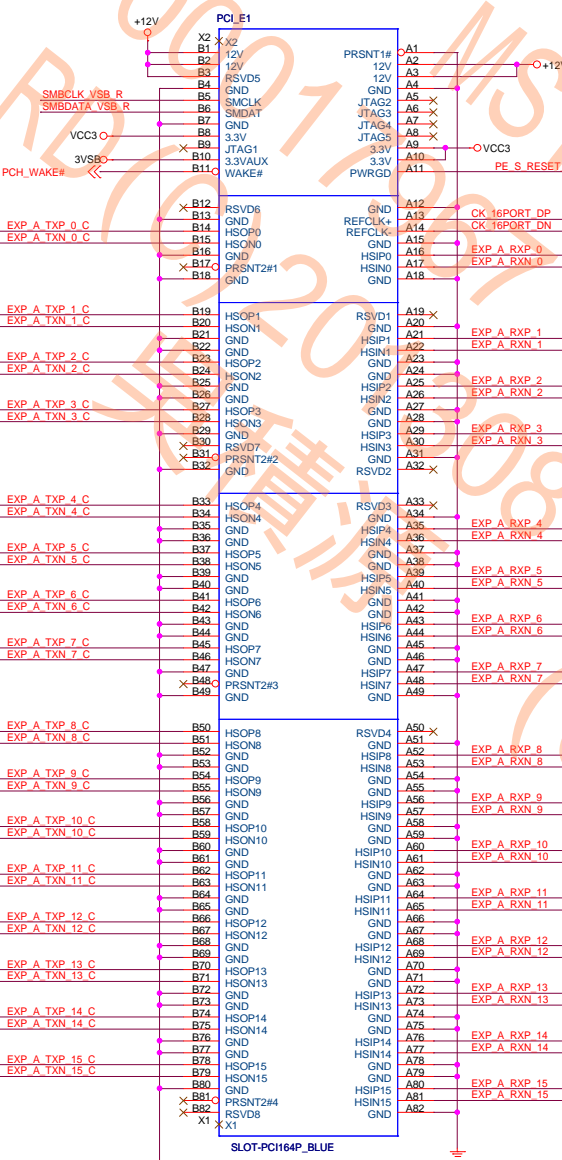


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11 SMBCLK_VSB_R
11 SMBDATA_VSB_R

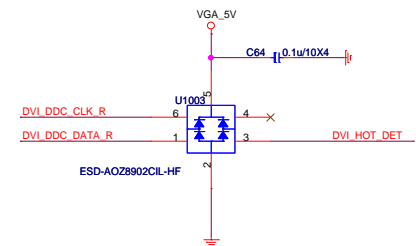
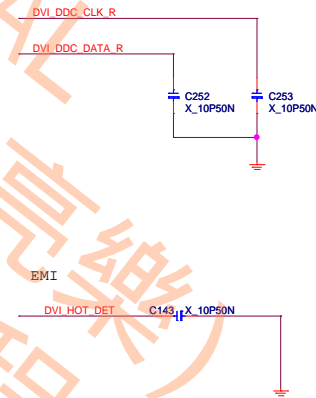
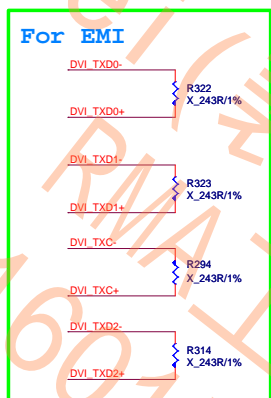
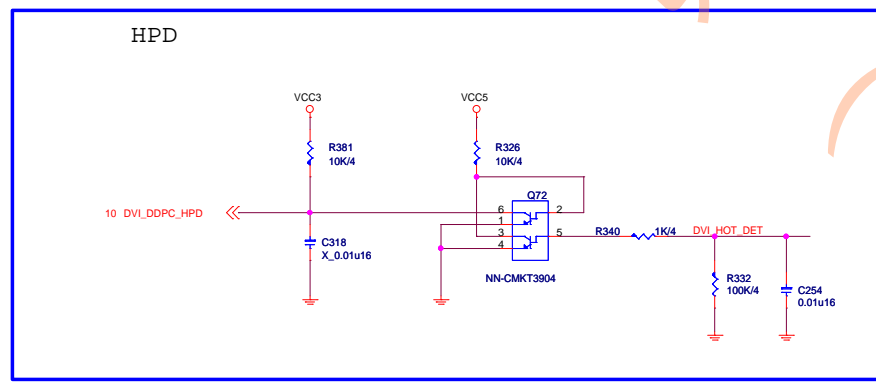
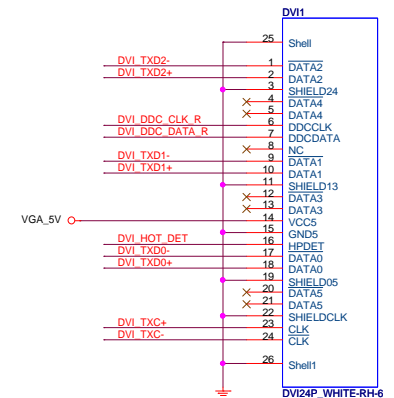
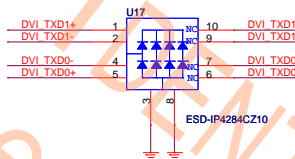
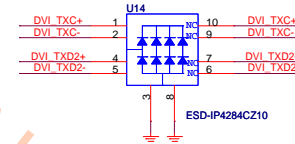
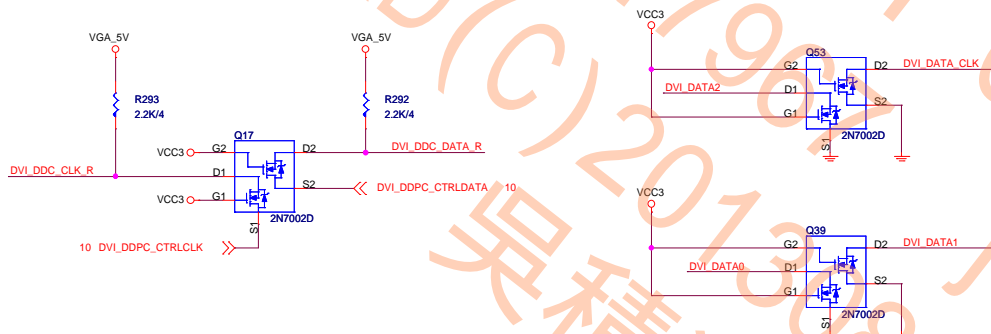


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DVI level shifter

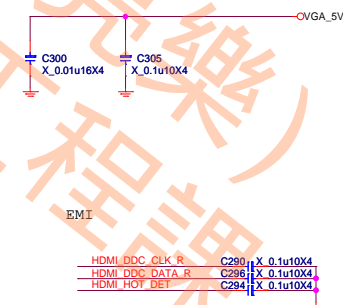
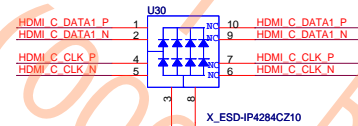
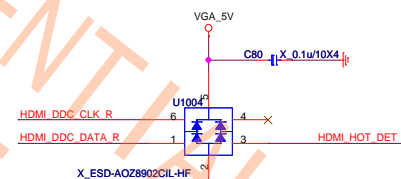
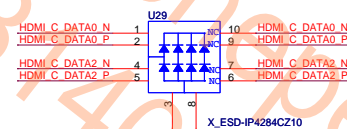
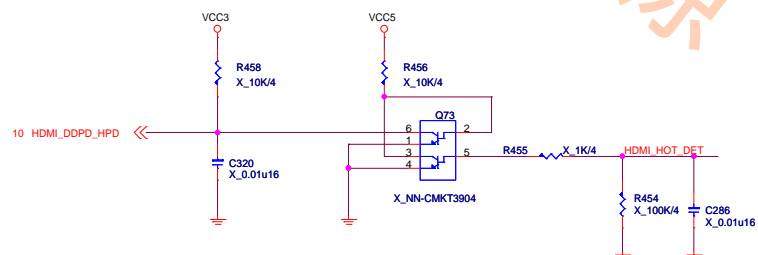
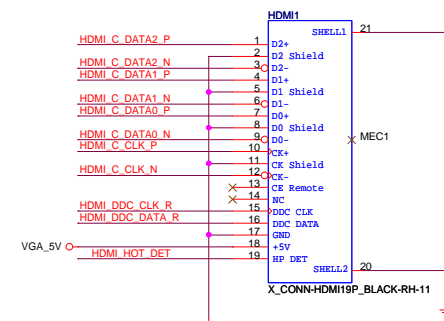
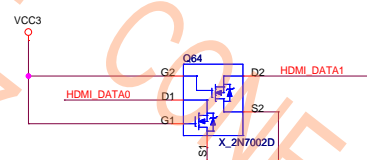
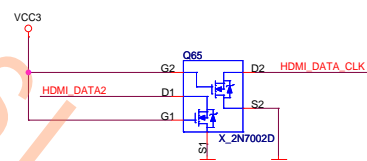
VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)

3	DVI_DDPG_CLK_N	C240	0.1u/10X4	DVI_TXC-	R280	470R1%0402	DVI_DATA_CLK
3	DVI_DDPG_CLK_P	C243	0.1u/10X4	DVI_TXC+	R281	470R1%0402	DVI_DATA_CLK
3	DVI_DDPG_TXN2	C251	0.1u/10X4	DVI_TXD2-	R283	470R1%0402	DVI_DATA2
3	DVI_DDPG_TXP2	C253	0.1u/10X4	DVI_TXD2+	R284	470R1%0402	DVI_DATA2
3	DVI_DDPG_TXN1	C250	0.1u/10X4	DVI_TXD1-	R287	470R1%0402	DVI_DATA1
3	DVI_DDPG_TXP1	C238	0.1u/10X4	DVI_TXD1+	R289	470R1%0402	DVI_DATA1
3	DVI_DDPG_TXN0	C222	0.1u/10X4	DVI_TXD0-	R281	470R1%0402	DVI_DATA0
3	DVI_DDPG_TXP0	C249	0.1u/10X4	DVI_TXD0+	R288	470R1%0402	DVI_DATA0



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3	HDMI_DDPD_CLK_P	C255	X 0.1u10X4	HDMI_C_CLK_P	R360	X 470R1%0402	
3	HDMI_DDPD_CLK_N	C270	X 0.1u10X4	HDMI_C_CLK_N	R359	X 470R1%0402	
3	HDMI_DDPD_CLK_X	C272	X 0.1u10X4	HDMI_C_DATA2_P	R380	X 470R1%0402	HDMI_DATA_CLK
3	HDMI_DDPD_TX2_P	C263	X 0.1u10X4	HDMI_C_DATA2_N	R384	X 470R1%0402	
3	HDMI_DDPD_TX2_N	C269	X 0.1u10X4	HDMI_C_DATA1_P	R392	X 470R1%0402	
3	HDMI_DDPD_TX1_P	C261	X 0.1u10X4	HDMI_C_DATA1_N	R388	X 470R1%0402	HDMI_DATA1
3	HDMI_DDPD_TX1_N	C259	X 0.1u10X4	HDMI_C_DATA0_P	R379	X 470R1%0402	
3	HDMI_DDPD_TX0_P	C257	X 0.1u10X4	HDMI_C_DATA0_N	R391	X 470R1%0402	HDMI_DATA0



HDMI_C.CLK_N

HDMI_C.CLK_P

R460

X_1/164/1/164

HDMI_C.DATA0_N

HDMI_C.DATA0_P

R468

X_1/164/1/164

HDMI_C.DATA1_N

HDMI_C.DATA1_P

R466

X_1/164/1/164

HDMI_C.DATA2_N

HDMI_C.DATA2_P

R469

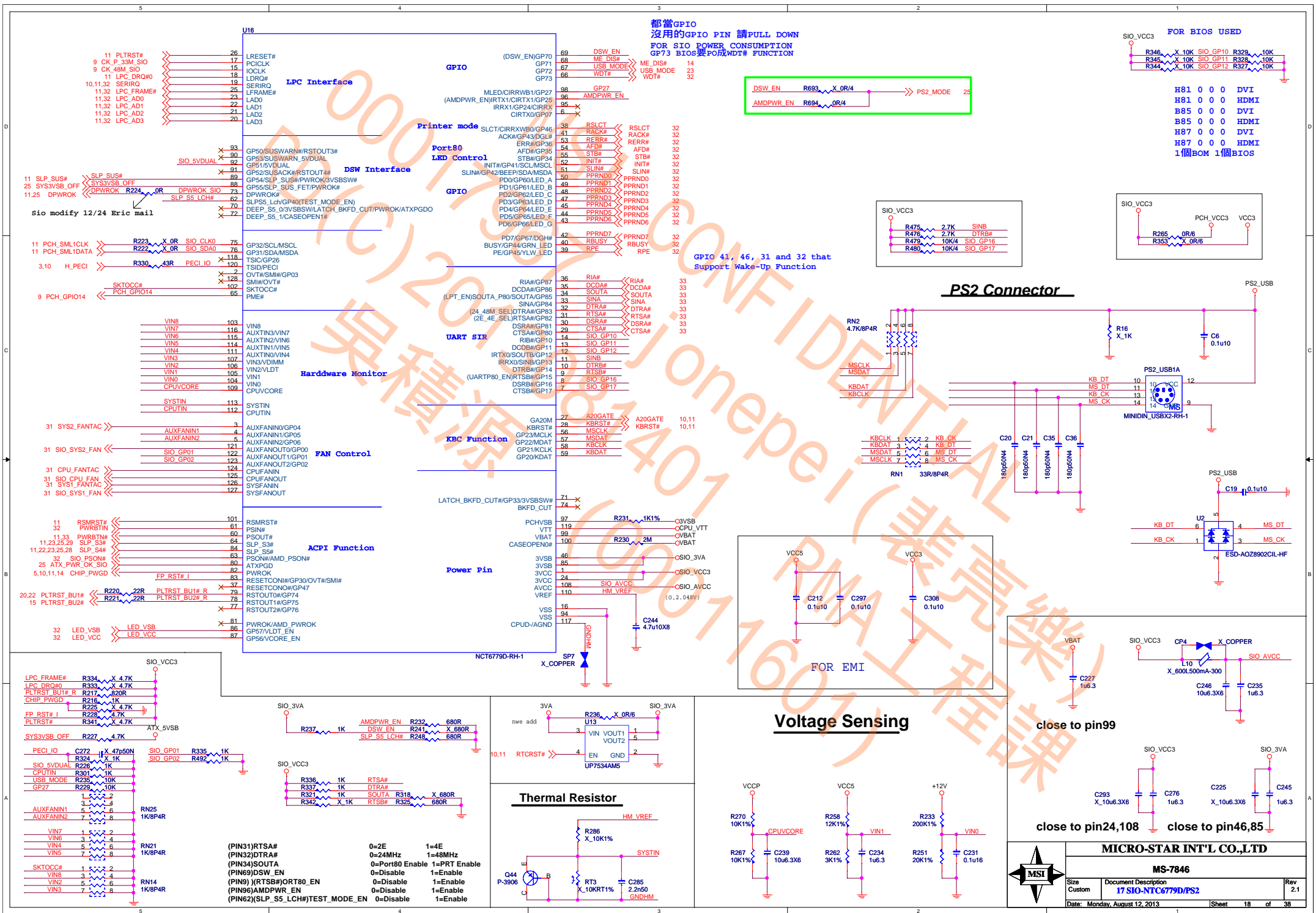
X_1/164/1/164



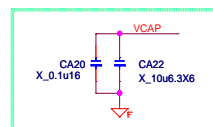
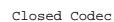
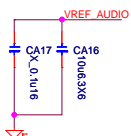
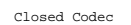
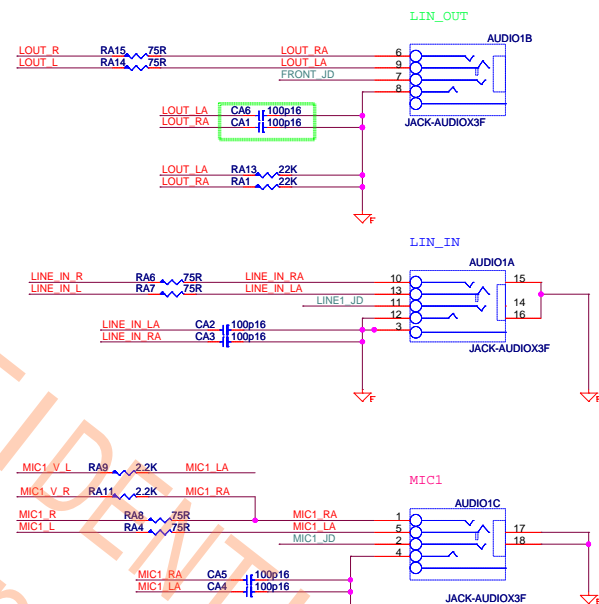
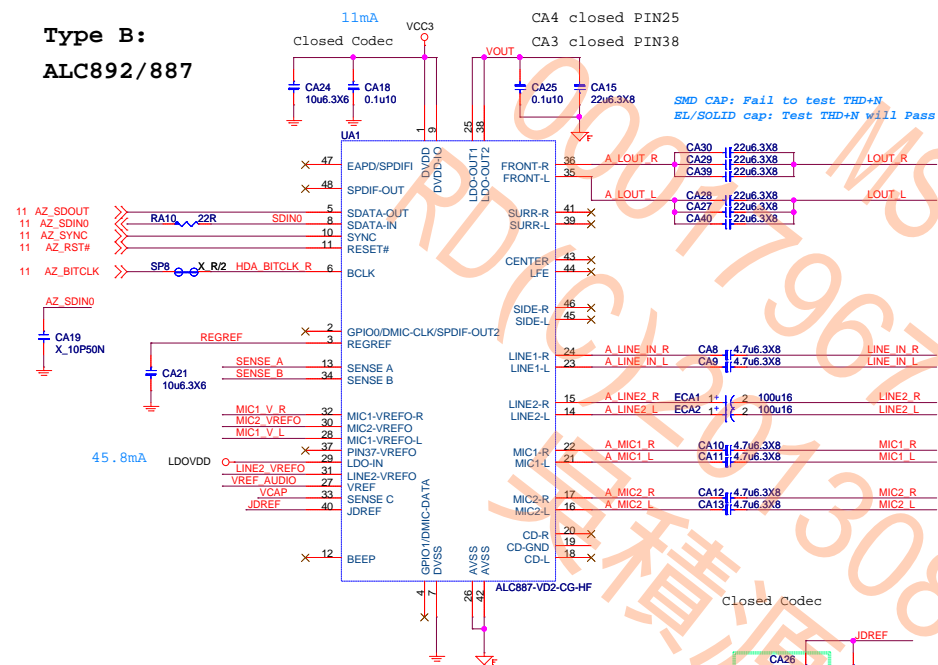
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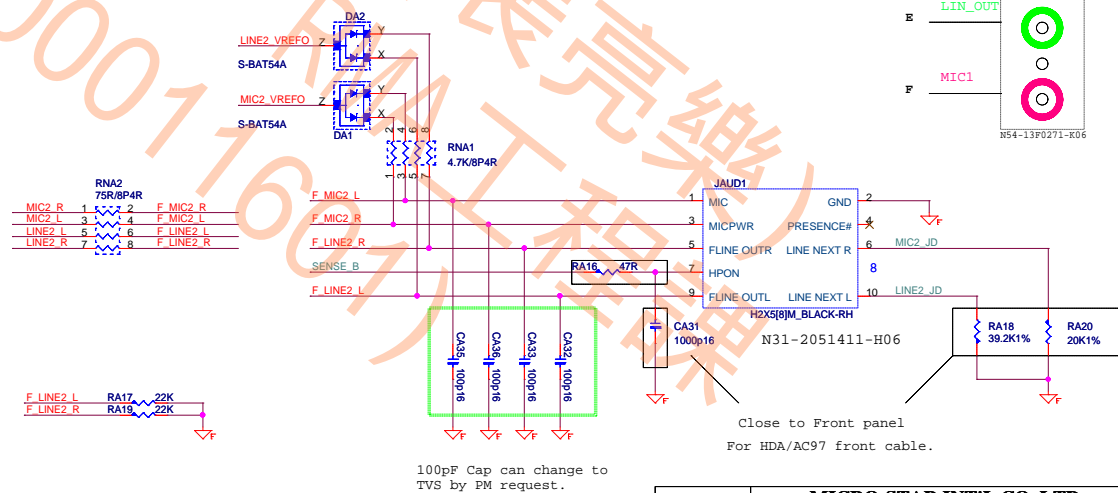
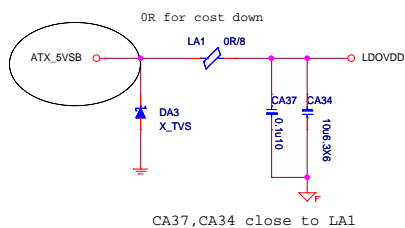
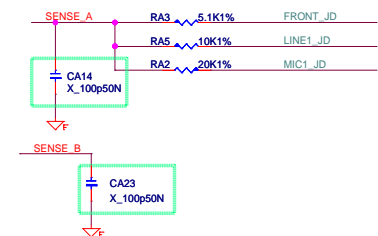
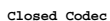
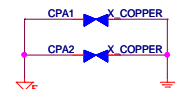
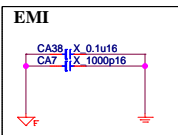
Sheet 17 of 38



Type B:
ALC892/887



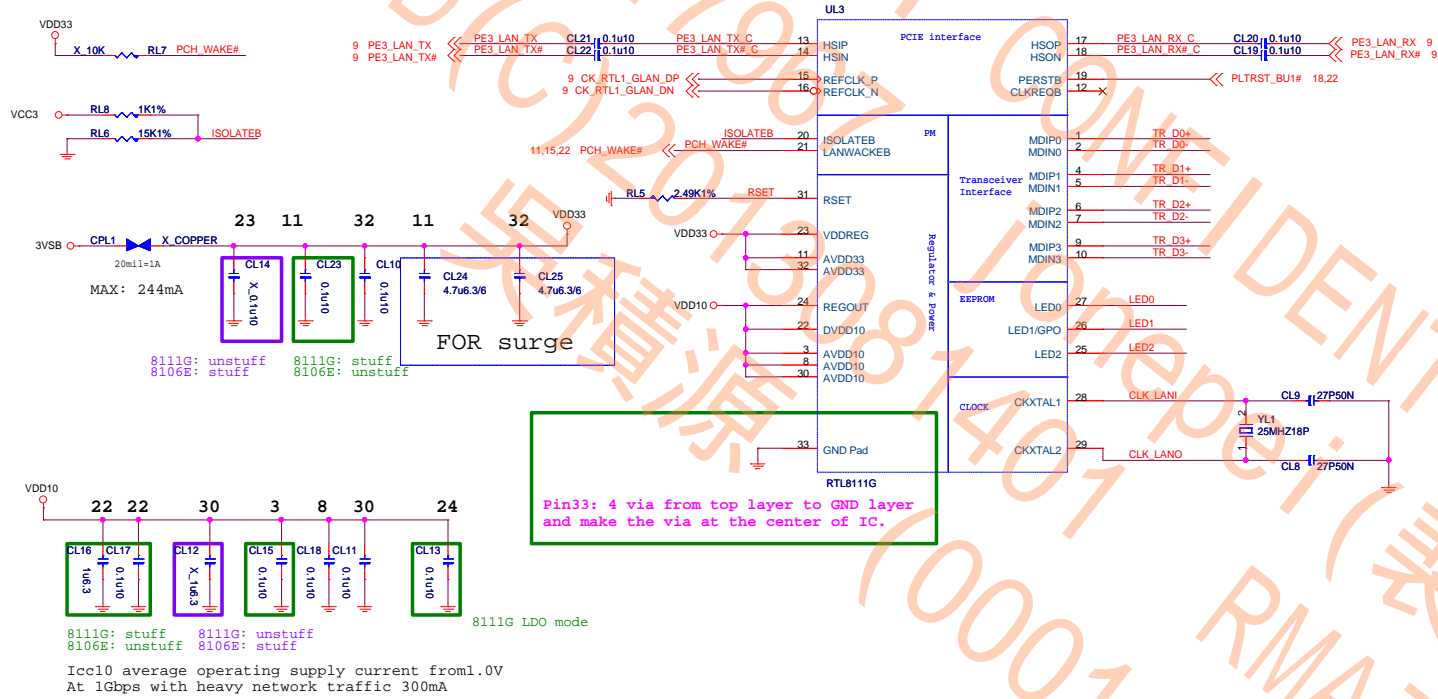
```
887: Remove
1708: Stuff
```



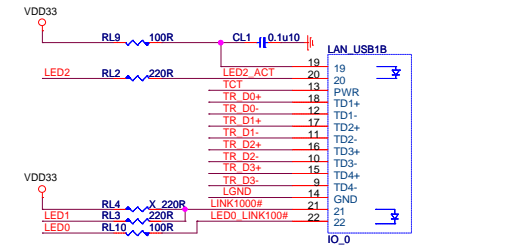
MICRO-STAR INT'L CO.,LTD			
MS-7846			
Size Custom	Document Description Audio Codec ALC892/887		Rev 2.1
Date: Monday, August 12, 2013		Sheet 19 of 38	

RTL8111G Giga LAN

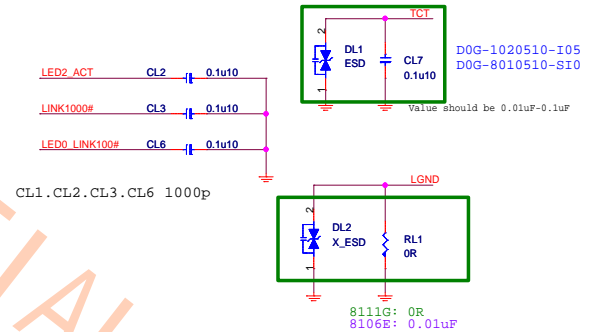
RTL8106E 10/100M LAN



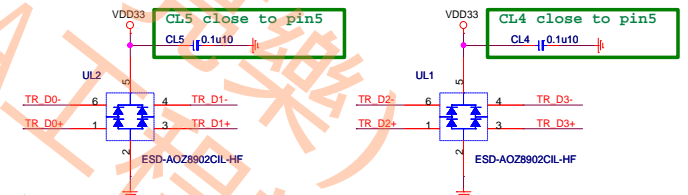
LAN Connector



8111G: Keep RL3 and Remove RL4 for RTL8111G
8106E: Keep RL4 and Remove RL3 for RTL8106E



Reserve ESD Protect



MSI P/N : D0G-0200529-A68, Vender P/N : AOZ8902CI
MSI P/N : D0G-0100619-I05, Vender P/N : TVLST2304AD0

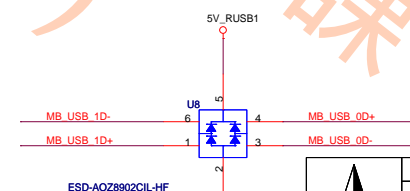
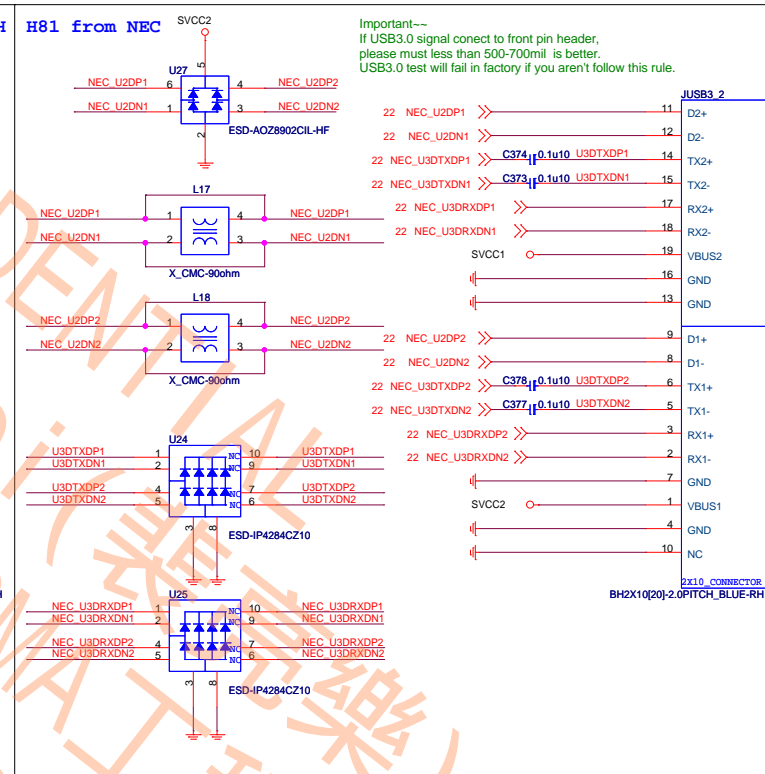
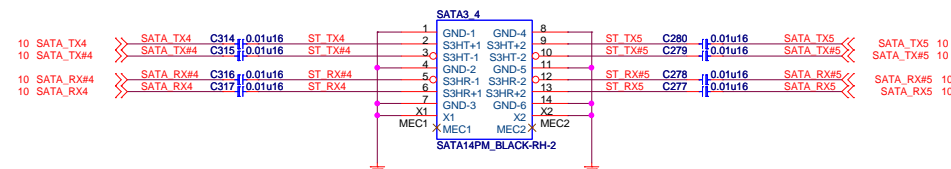
8106E POWER Consumption

	3.3V @ mA	mW
10 M Idle/TxRx	15/94	49.5/310.2
100 M Idle/TxRx	52/105	171.6/346.5
S0 ALDPS	4	13.2

8111G POWER Consumption

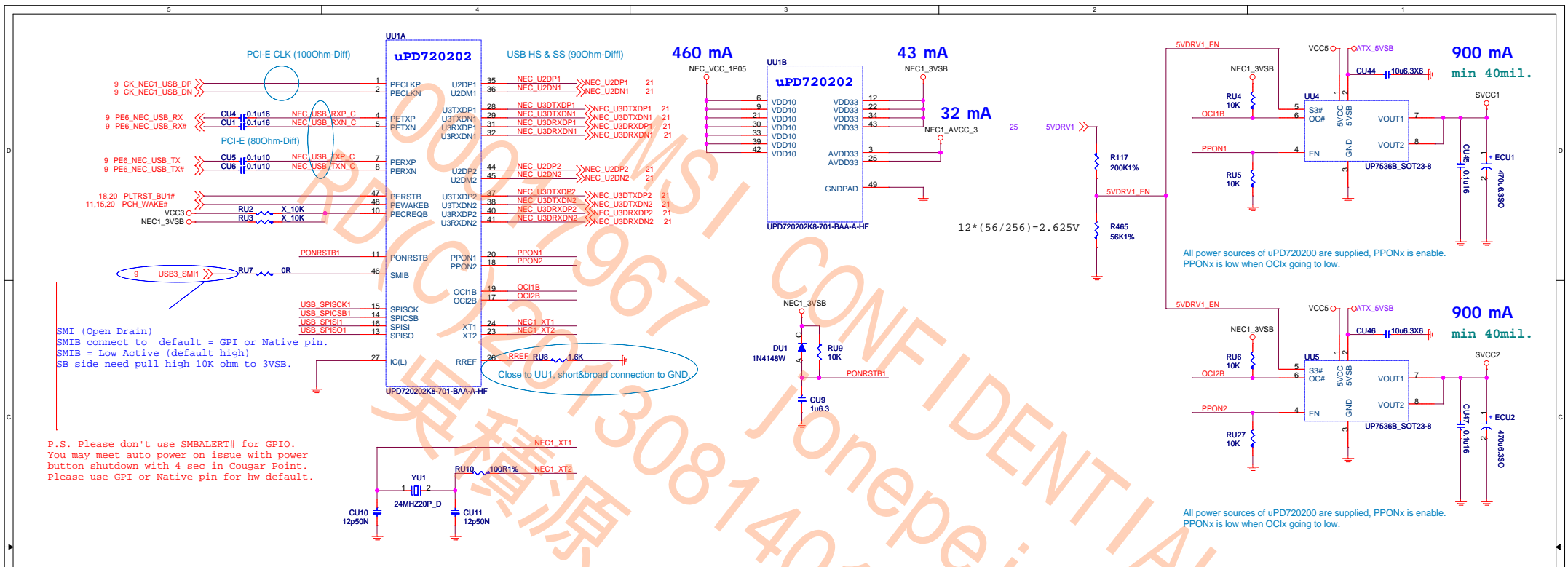
	3.3V @ mA	mW
10 M Idle/TxRx	17.15/116.7	56.6/385.1
100 M Idle/TxRx	71.45/129.5	235.8/427.4
Giga Idle/TxRx	179.1/243.9	591/804.9
ALDPS	6.41	21.15

SATA 3G PORT 4,5

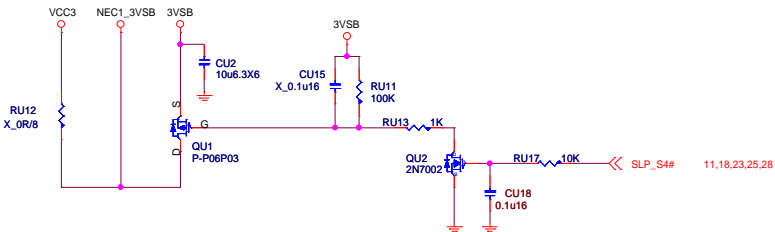


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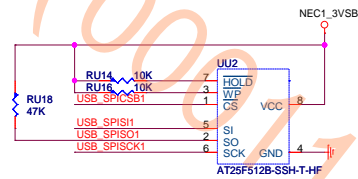
Size Custom	Document Description SATA Connector	Rev 2.1
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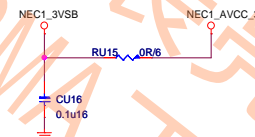
3V_Dual Circuit



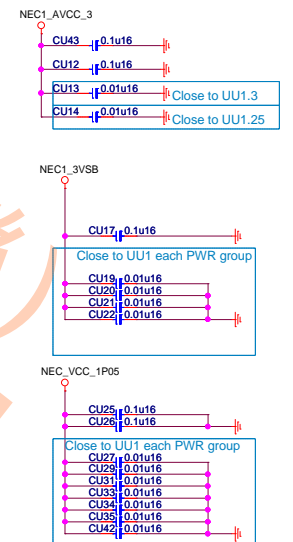
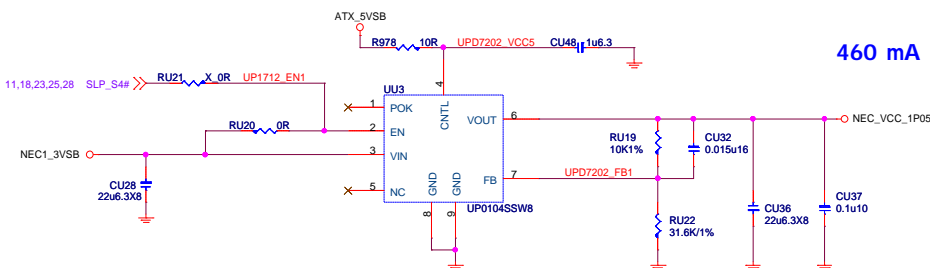
EEPROM



AVCC3 STB Power



uPD720200 core Power



MICRO-STAR INT'L CO.,LTD

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Size	Document Description	Rev
Custom	Renesas uPD720202 USB3.0 2PORT	2.1
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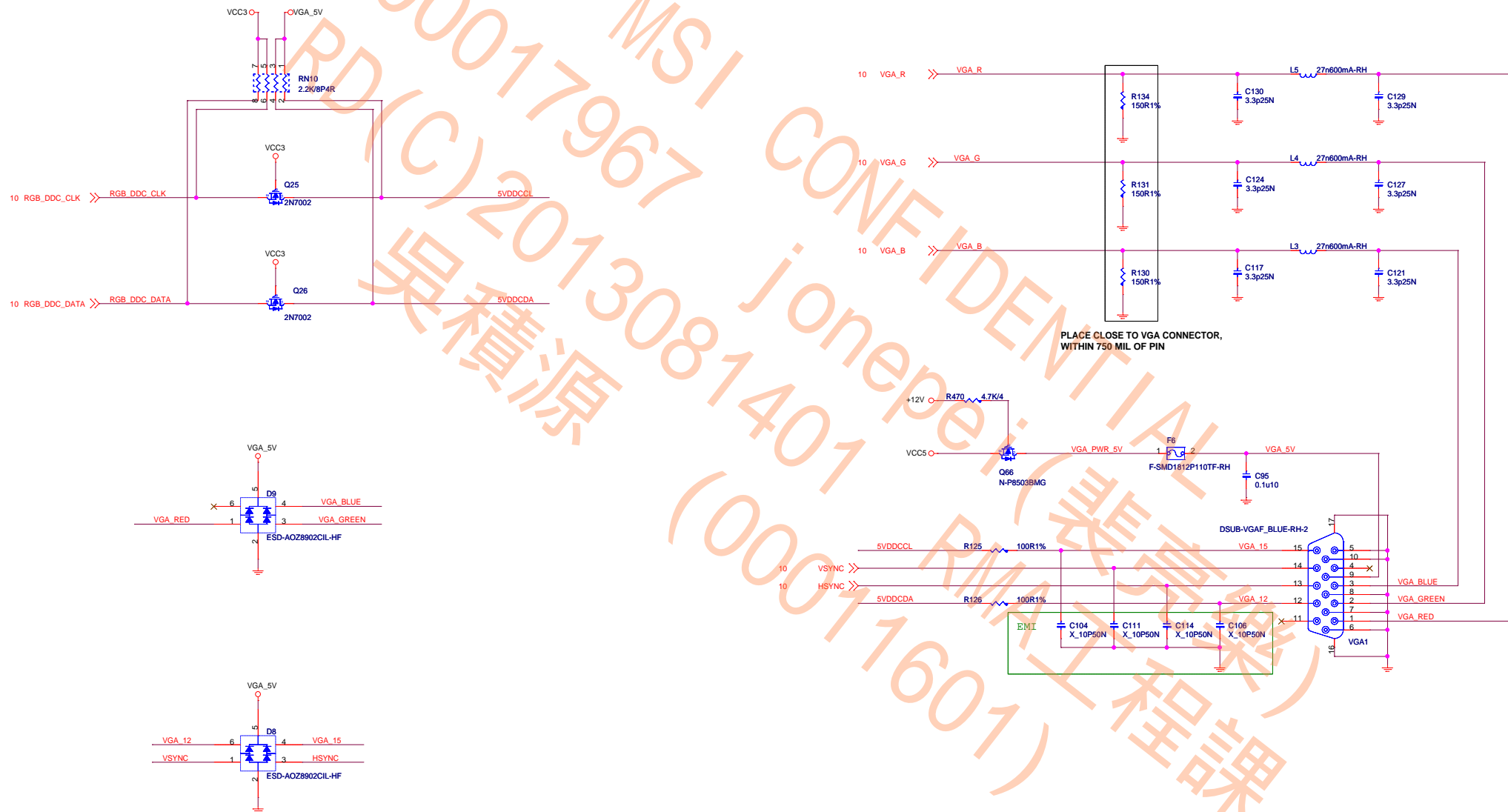
PCH/FCH side: OC# pull high to +3VSB

D08-2000300-P16 (Itrip=3.5A; 0.003ohm) support 6 USB ports (3A)
D08-0300700-P16 (Itrip=2.6A; 0.015ohm) support 4 USB ports (2A)
D08-0100110-P16 (Itrip=1.1A; 0.04ohm) support 2 USB ports (1A)
D08-2000200-P16 (Itrip=3.5A; 0.003ohm) MINISMD050



D-Sub

Level shift



MICRO-STAR INT'L CO.,LTD

MS-7846

Size
Custom

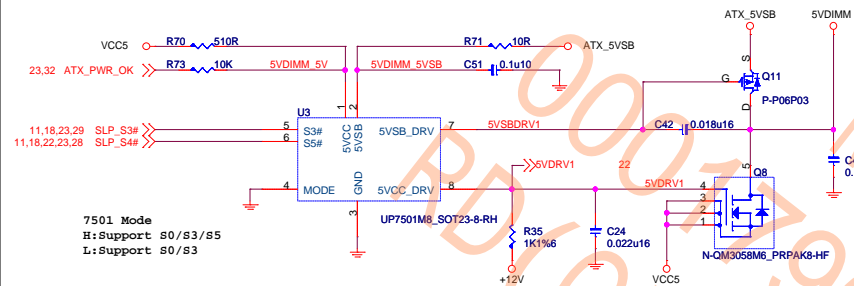
Document Description
VGA Connector

Rev	2.1
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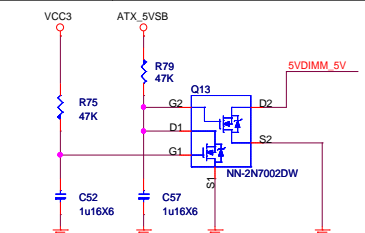
Date: Monday, August 12, 2013

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5VDIMM FOR DDR



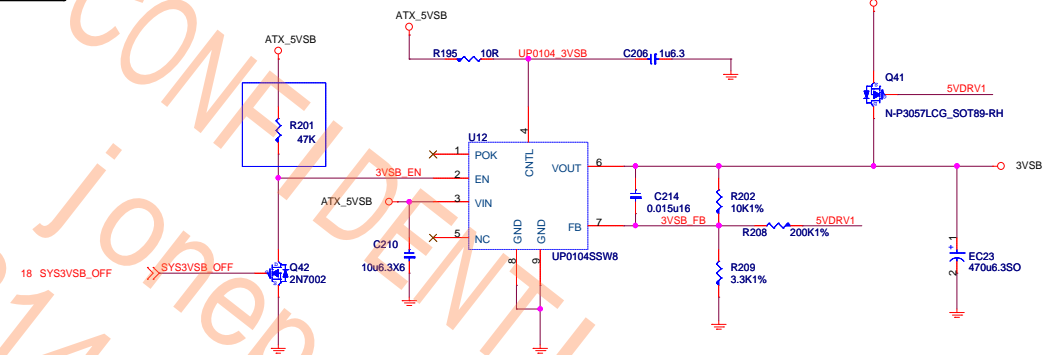
For power 700W solution (only for uP7501+uP7506 for 3VSB solution)
The power supply VCC3 delay 12ms after VCC5 assert.
The chip U7501 5VDRV1 work when the VCC5 ready
(When VCC5 up to 4.2V and the 5VDRV1 delay 6ms assert), but
VCC3 not ready and let the 3VSB sequence fail.



Patch coolermaster 700w power sequence

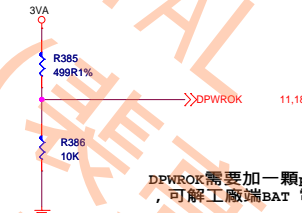
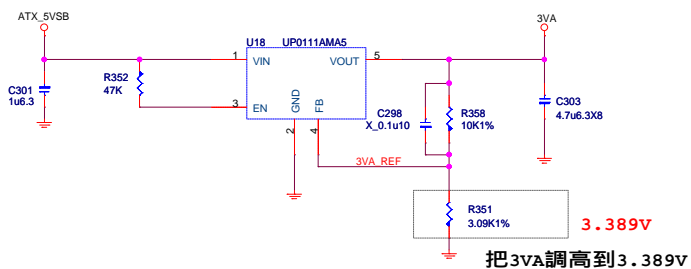
3VSB

3VSB supply to PCH and other device.
Turn off when Deep S3/S5 by 5VSB off.



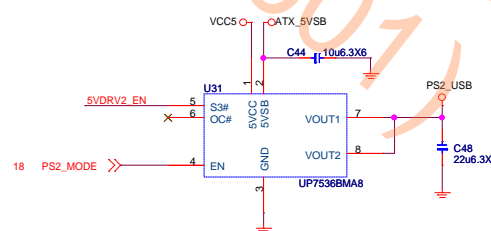
3VA

20mA



DPWROK需要加一顆pull down 10k電阻
，可解工廠端BAT 電流過大問題

PS2 Power



USB MODE

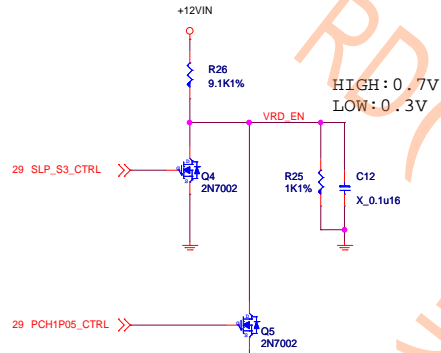


MICRO-STAR INT'L CO.,LTD

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Size	Document Description	Rev
Custom	ACPI controller UPI	2.1
Date: Monday, August 12, 2013	Sheet 25 of 38	

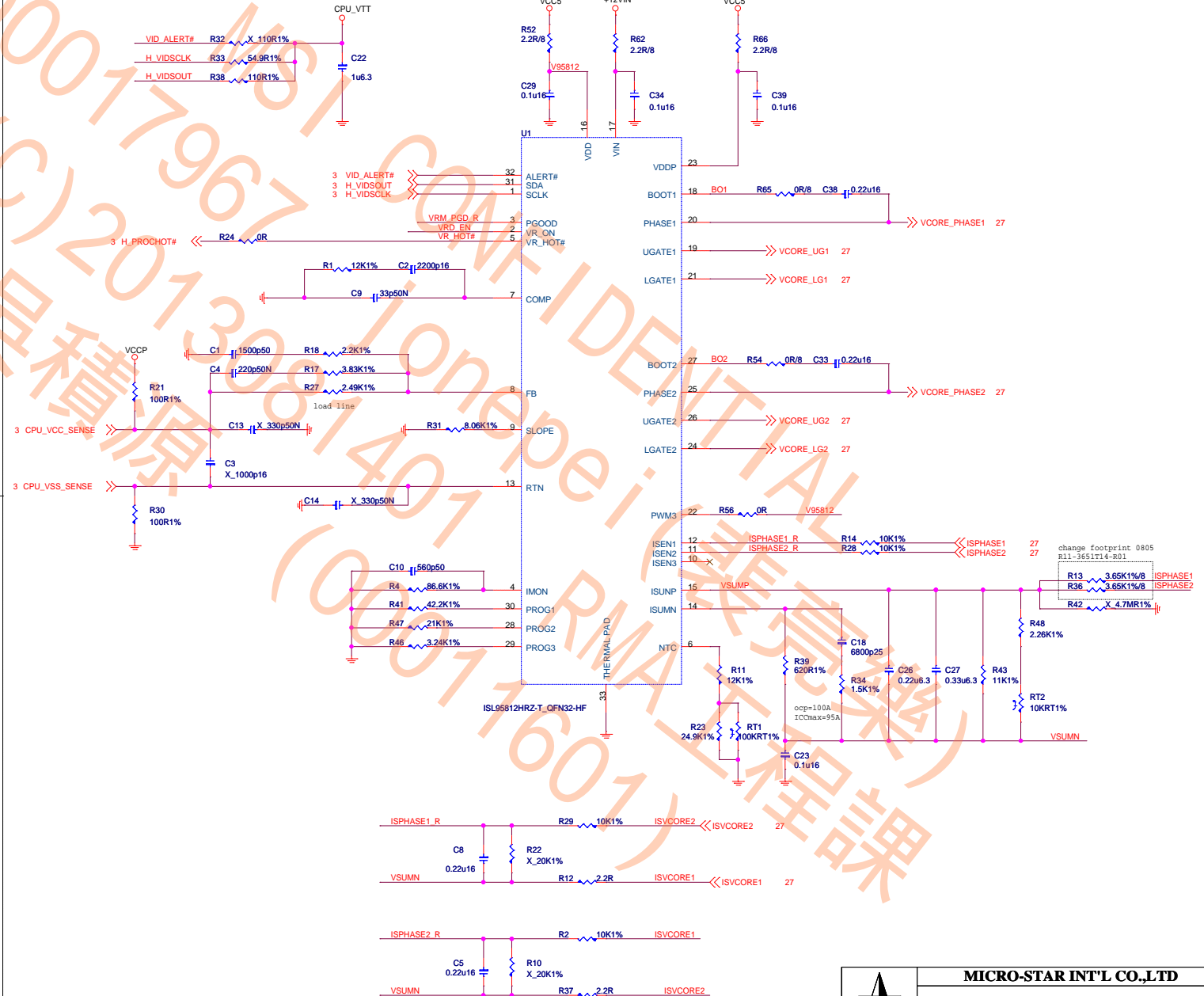
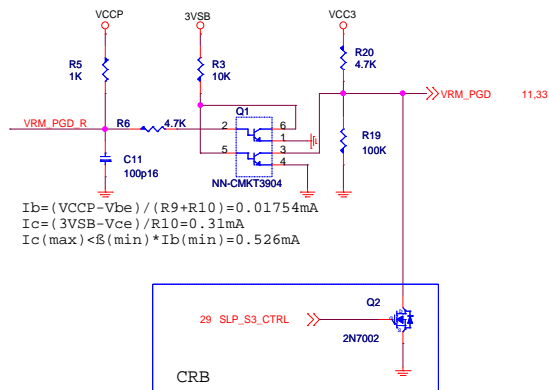
VCORE power on by s3 and 12v



CRB

HIGH:by PCH_1P05V
LOW:by S3

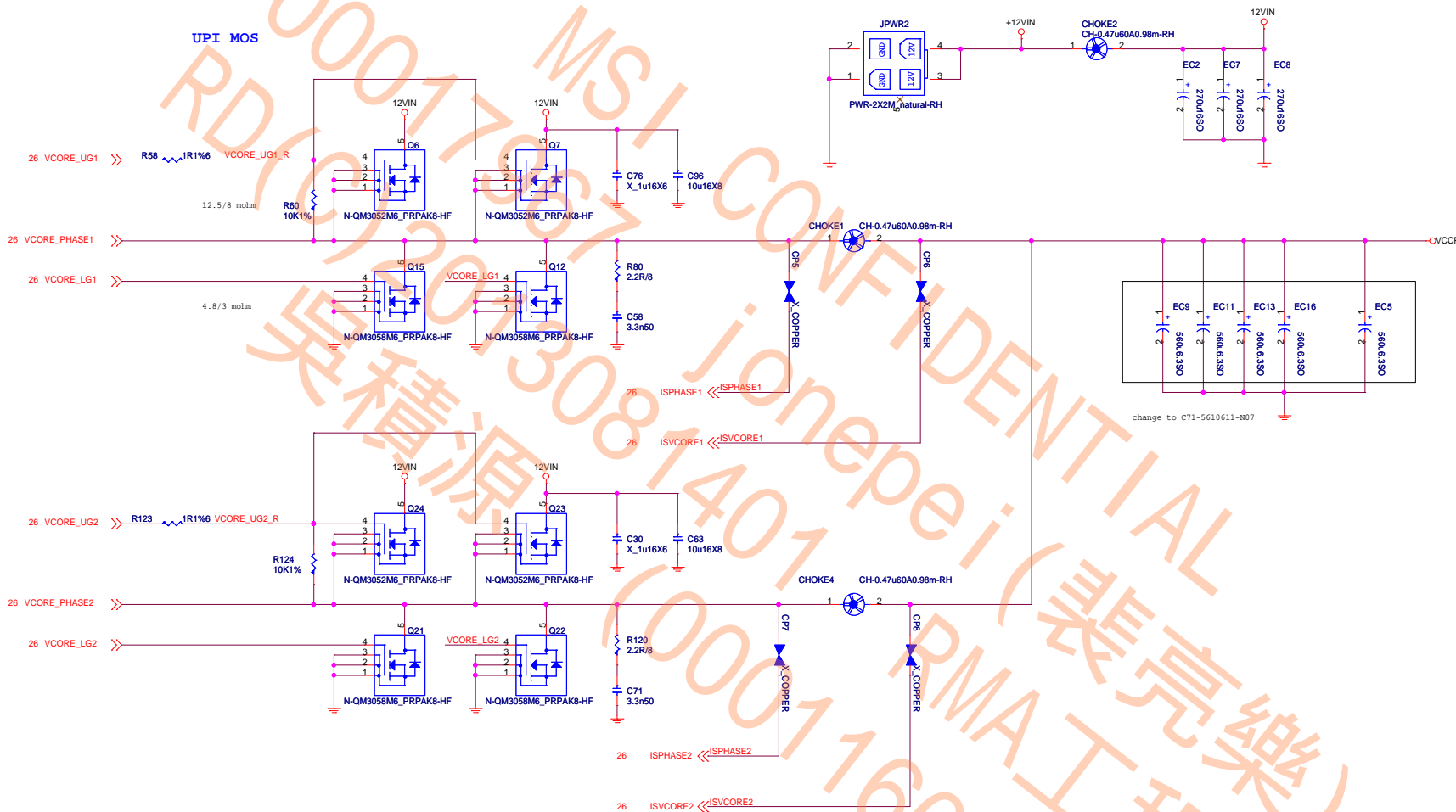
VRMPWRGD LEVEL SHIFT



VCCP POWER

VCORE ICC MAX70A ICCTDC:47A 65W
LL:2.5m ohm

Irms_input=17.5A



MICRO-STAR INT'L CO.,LTD

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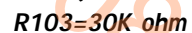
Size Custom

Document Description
VCCP POW

Date: Monday August 12 2013

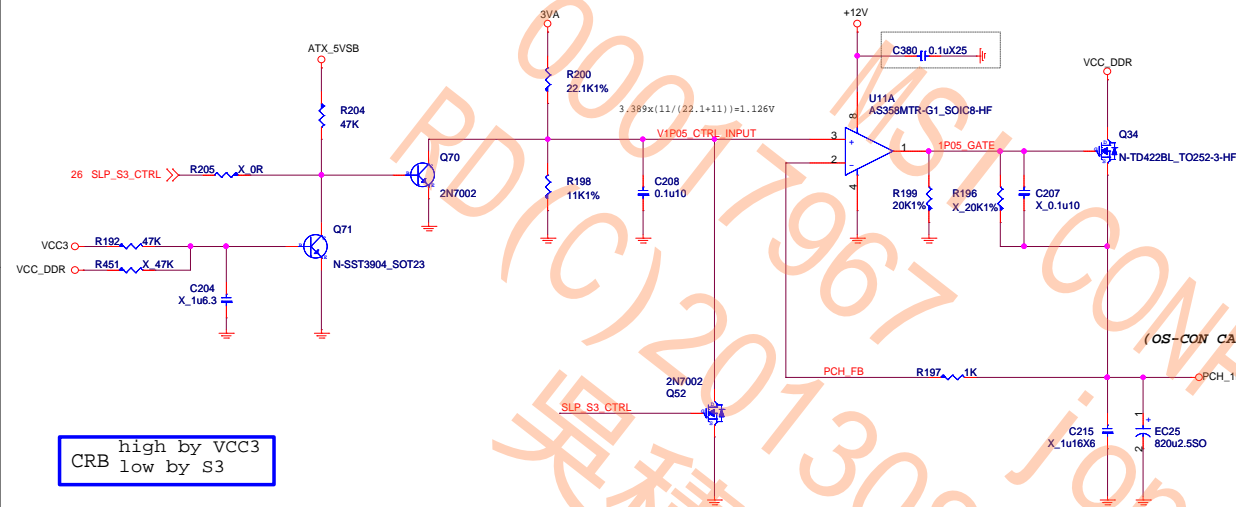
Sheet 27 of 38

5.747A FOR PCH

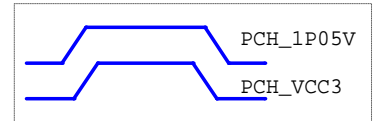
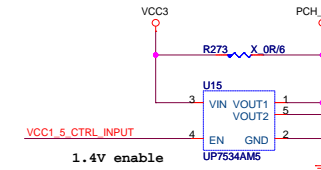


Size Custom	Document Description DDR Power -UP6103 1-Phase	Rev 2.1
Date: Monday, August 12, 2013		Sheet 28 of 38

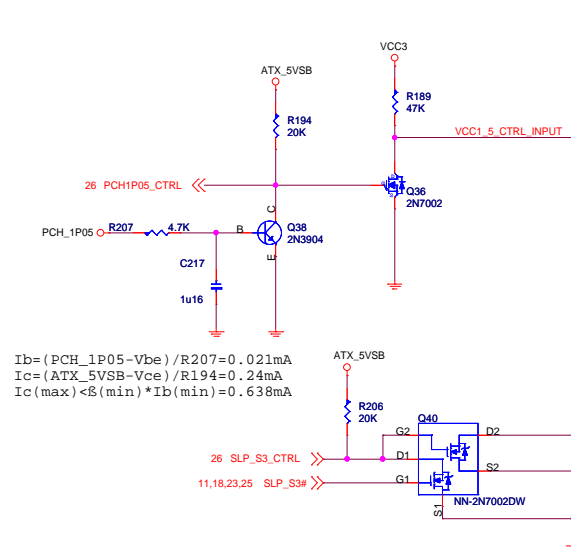
PCH Power:1.05V 5.747A



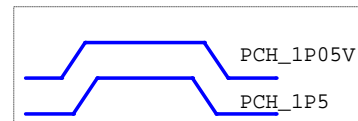
0.133A



PCH Power:1.5V 0.183A



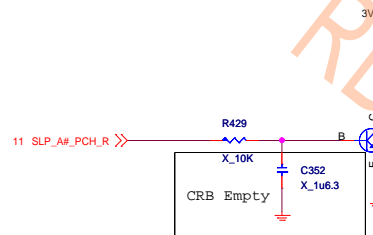
VCC1_5_CTRL_INPUT:
0:1P05V low or S3 low
1:1P05V HIGH and S3 HIGH



	MICRO-STAR INT'L CO.,LTD		
	MS-7846		
Size	Document Description	Rev	
Custom	PCH Power - OP+MOS	2.1	
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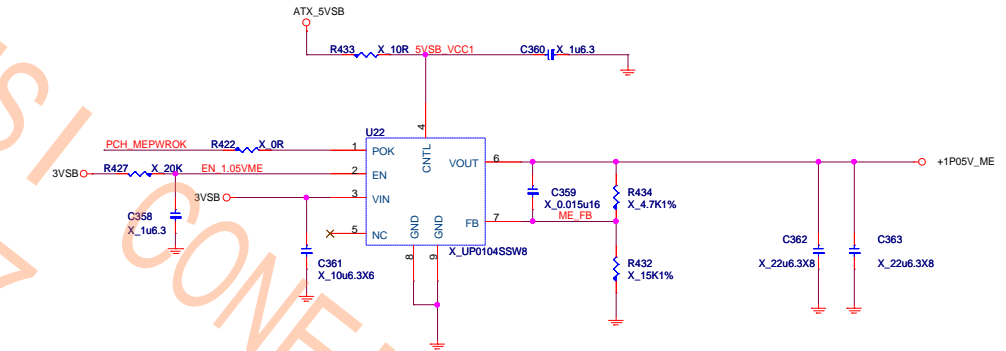
PCH ME Power:1.05V 0.670A

SLP_A

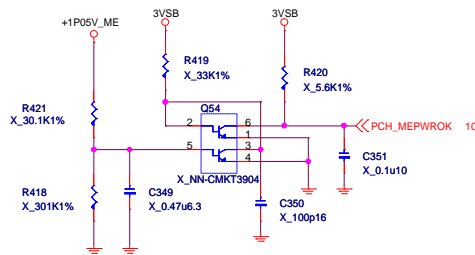


SLP_A#_PCH_R R430 X_0R EN_1.05VME

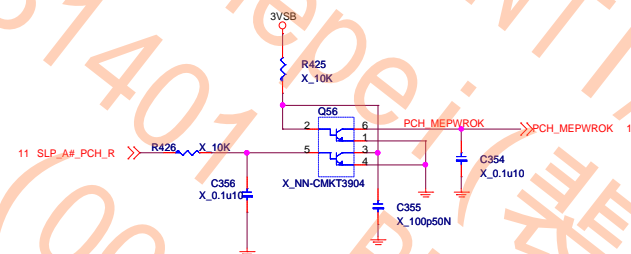
ME Power Control



PCH_MEPWROK

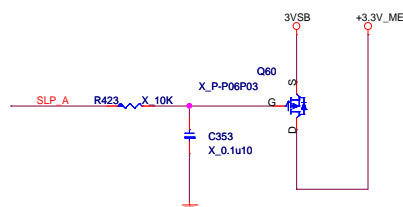


VccASW active to APWROK high 1ms



APWROK falling to VccASW falling 40ns

+3.3V_ME



For INTEL ME



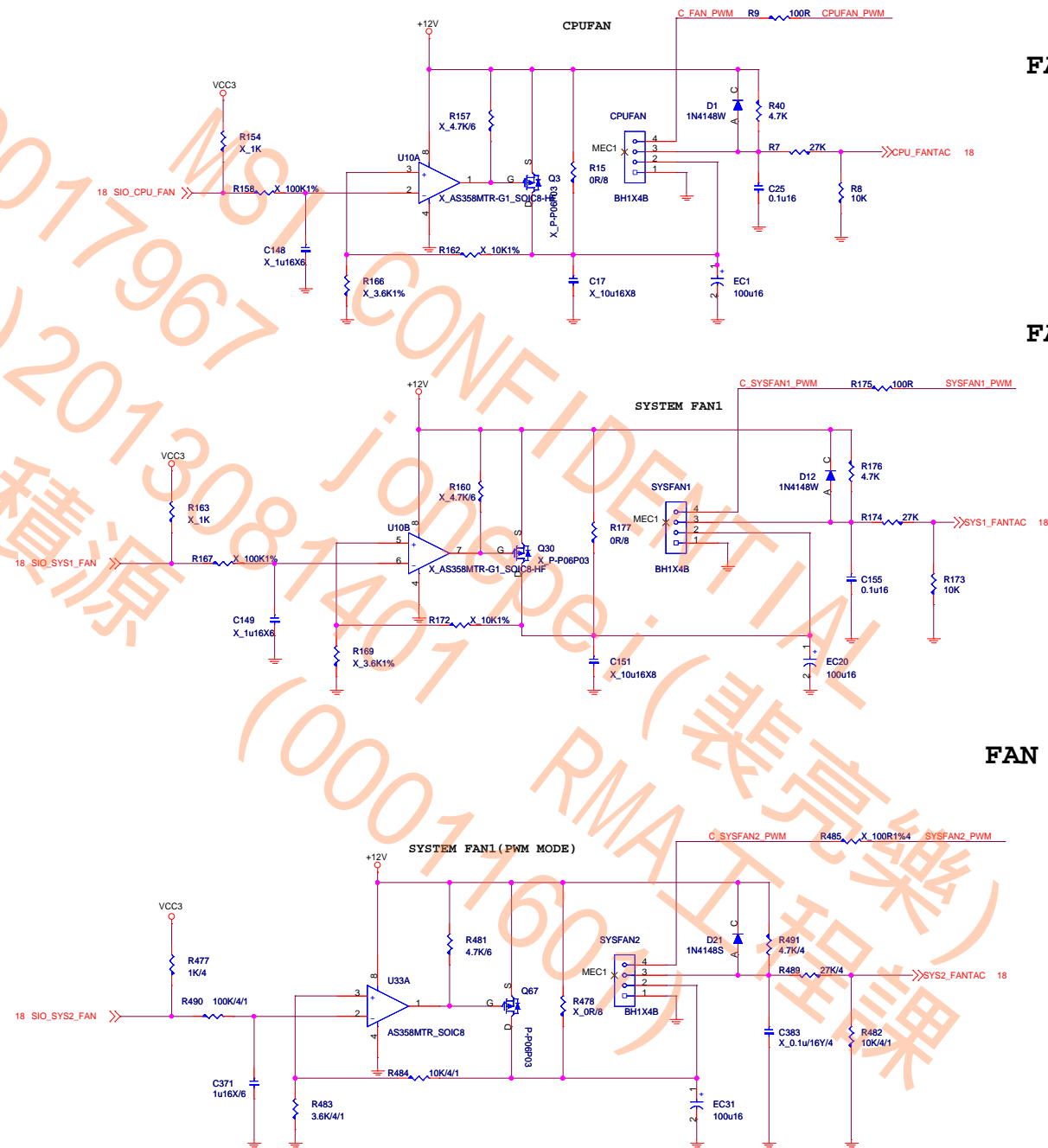
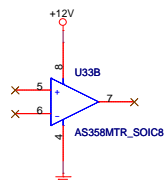
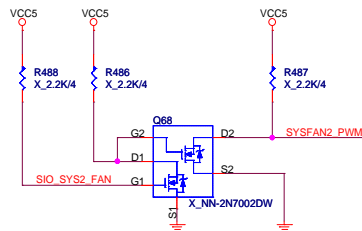
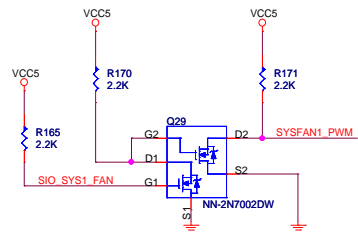
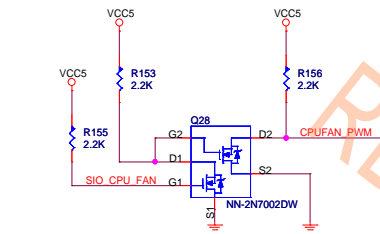
H81 stuff R424
B85 stuff R444

FAN-COUNTROL CIRCUIT

FAN TYPE E

FAN TYPE E

FAN TYPE F



[illegible][illegible]

Pin 10-18 connector diagram for H2XT10M-2PITCH_BLACK-RH. The diagram shows a 14-pin connector with pins numbered 1 to 14. Pin 1 is labeled JTPM1. Pin 2 is labeled 3VSB. Pin 3 is labeled TPM_CLK. Pin 4 is labeled PE_S RESET_N. Pin 5 is labeled LPC_ADO0. Pin 6 is labeled OVCC3. Pin 7 is labeled LPC_ADO1. Pin 8 is labeled OVCC5. Pin 9 is labeled LPC_ADO2. Pin 10 is labeled SERIRQ. Pin 11 is labeled LPC_ADO3. Pin 12 is labeled LPC_FRAME#. Pin 13 is labeled LPC_FRAME#. Pin 14 is labeled LPC_FRAME#. The diagram also shows a 3VSB power supply connection to pin 2 and a ground connection to pin 14.

PARALLEL PORT

VCC5 ○ D6_A ○ C89 LPT1 VC

C79 0.1u10

RN6 33R/8P4R

PRND0 8 7 PRND0 2 1

PRND1 6 5 PRND1 4 3

PRND2 4 3 PRND2 6 5

PRND3 2 1 PRND3 8 7

RN4 33R/8P4R

PRND4 8 7 PRND5 4 3

PRND5 6 5 PRND6 6 5

PRND6 4 3 PRND7 8 7

PRND7 2 1

RN8 33R/8P4R

AFD# 8 7 RAFD# 2 1

STB# 6 5 RSTB# 4 3

INIT# 4 3 RINIT# 6 5

SLIN# 2 1 RSLIN# 8 7

RN3 2.7K/8P4R

RACK# 2 1

RBUSY 4 3

RPE 6 5

RSLCT 8 7

RERR# R122 2.7K

VCC5 ○ C87 0.1u10

RSTB# 14 RAFD# 14

PRND0 2 15 RERR# 16

PRND1 3 16 RINIT# 17

PRND2 4 17 RSLIN# 18

PRND3 5 18

PRND4 6 19

PRND5 7 20

PRND6 8 21

PRND7 9 22

RACK# 10 23

RBUSY 11 24

RPE 12 25

RSLCT 13 26

DSU

18

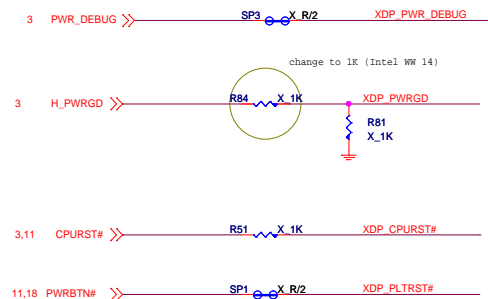
11,14



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Rev	2.1
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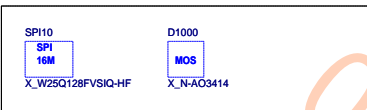
Date: Monday, August 12, 2013	Sheet 32 of 38
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[illegible][illegible]

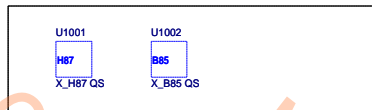
MS-7846

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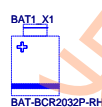
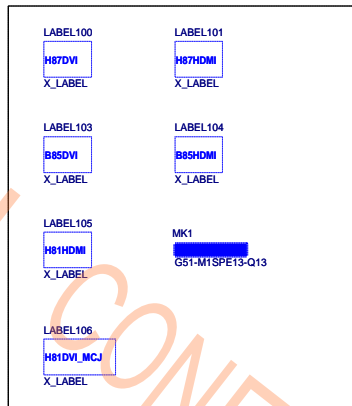
SPI OPT.



CHIPSET OPT.



LABEL OPT.

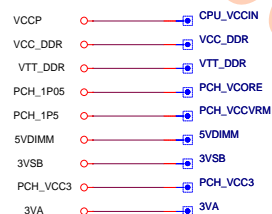
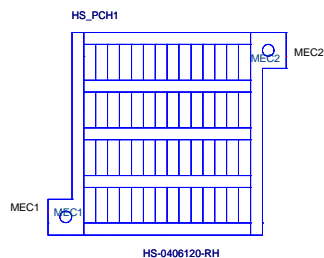


7846_21
PK0-0784621-G37
PK0-0784621-E48

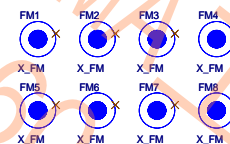
Simulation



PCH XDP PWRGD/RESET



Optical Fiducial Marks-120



Mounting Holes

